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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,658	02/09/2004	Yoichi Tamaki	XA-10036	7635
181 7590 04/08/2008 MILES & STOCKBRIDGE PC 1751 PINNACLE DRIVE SUITE 500 MCLEAN, VA 22102-3833				
EXAMINER				
PHAM, LONG				
ART UNIT		PAPER NUMBER		
2814				
NOTIFICATION DATE		DELIVERY MODE		
04/08/2008		ELECTRONIC		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ipdocketing@milestockbridge.com  
sstiles@milestockbridge.com

### Office Action Summary

**Application No.**

10/773,658

**Applicant(s)**

TAMAKI ET AL.

**Examiner**

Long Pham

**Art Unit**

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SF 298)  
Paper No(s)/Mail Date \_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_

### DETAILED ACTION

#### ***Claim Rejections - 35 USC § 103***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takashi et al. (Japan 2002-057219) in combination with Kinoshita (US pat 6,300,669), Kitahara et al. (US pat 4948748) and Moyer (US patent 5,374,844).

With respect to claim 1, Takashi et al. a semiconductor device comprising (see figs. 1-6 and English abstract):

- a) a semiconductor layer 3 that is provided over a layer (a p-n junction at the interface between 2 and 3) of electrically insulating material (since the p-n junction electrically insulates the bipolar transistors);
- b) a plurality of first bipolar transistors 18,19 are provided on the semiconductor layer ; and
- c) an first isolation 4-1, 4-4 is provided over a main surface of the semiconductor layer to reach the layer of electrically insulating material, wherein at least a portion of the plurality of bipolar transistors are surrounded by the layer of electrically insulating material and the isolation, and wherein the surrounded transistors would inherently operate substantially uniformly as constituent elements of a unit transistor.

Takashi et al. fail to teach that the collectors, emitters, and bases of the bipolar transistors are respectively connected in parallel with each other.

Kinoshita teaches collectors, emitters, and bases of a plurality of bipolar transistors are respectively connected in parallel with each other to achieve low-noise, high-power gain high frequency amplifier. See claim 1 and abstract.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Kinoshita into the device of Takashi et al. to attain the above benefit.

Further with respect to claim 1, Takashi et al. teach the electrically insulating layer is made of np junction layer but fail to teach the electrically insulating layer is

made of material having lower thermal conductivity than the semiconductor layer or oxide.

Kitahara et al. teach using an oxide 13 to provide effective isolation for bipolar transistors.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Kitahara et al. into the device of Takashi et al. to attain the above benefit.

With respect to claims 2 and 3, Takashi et al. further fail to teach each of emitter of the plurality of bipolar transistors is connected to a resistor made of polysilicon.

Moyer teaches connecting a polysilicon resistor to an emitter of a bipolar transistor to prevent thermal runaway. See col. 1, lines 35-40.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Moyer into the device of Takashi et al. to attain the above benefit.

With respect to claims 4 and 5, Takashi et al. implicitly teach collector and base contact holes but fail to teach the range for the distance between contact holes for the base and collector of plurality of first and second bipolar transistors.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the distance between contact holes for the base and collector through routine experimentation and optimization to obtain optimal or desired device performance because in the absence of unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takashi et al. (Japan 2002-057219) in combination with Kinoshita (US pat 6,300,669), Kitahara et al. (US pat 4948748) and Moyer (US patent 5,374,844).

With respect to claim 6, Takashi et al. a semiconductor device comprising (see figs. 1-6 and English abstract):

a) a semiconductor layer 3 that is provided over a layer (a p-n junction at the interface between 2 and 3) of electrically insulating material (since the p-n junction electrically insulates the bipolar transistors);

b) a plurality of first bipolar transistors 18,19 are provided on the semiconductor layer ; and

c) an first isolation 4-1, 4-4 is provided over a main surface of the semiconductor layer to reach the layer of electrically insulating material, wherein at least a portion of the plurality of bipolar transistors are surrounded by the layer of electrically insulating material and the isolation, and wherein the surrounded transistors would inherently operate substantially uniformly as constituent elements of a unit transistor.

Takashi et al. fail to teach that the collectors, emitters, and bases of the bipolar transistors are respectively connected in parallel with each other.

Kinoshita teaches collectors, emitters, and bases of a plurality of bipolar transistors are respectively connected in parallel with each other to achieve low-noise, high-power gain high frequency amplifier. See claim 1 and abstract.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Kinoshita into the device of Takashi et al. to attain the above benefit.

Further with respect to claim 6, Takashi et al. teach the electrically insulating layer is made of np junction layer but fail to teach the electrically insulating layer is made of material having lower thermal conductivity than the semiconductor layer or oxide.

Kitahara et al. teach using an oxide 13 to provide effective isolation for bipolar transistors.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Kitahara et al. into the device of Takashi et al. to attain the above benefit.

With respect to claims 6 and 7, Takashi et al. further fail to teach each of emitter of the plurality of bipolar transistors is connected to a resistor made of polysilicon.

Moyer teaches connecting a polysilicon resistor to an emitter of a bipolar transistor to prevent thermal runaway. See col. 1, lines 35-40.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Moyer into the device of Takashi et al. to attain the above benefit.

With respect to claims 8 and 9, Takashi et al. implicitly teach collector and base contact holes but fail to teach the range for the distance between contact holes for the base and collector of plurality of first and second bipolar transistors.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the distance between contact holes for the base and collector through routine experimentation and optimization to obtain optimal or desired device performance because in the absence of unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Claims 10-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takashi et al. (Japan 2002-057219) in combination with Kinoshita (US pat 6,300,669), Kitahara et al. (US pat 4948748) and Moyer (US patent 5,374,844).

With respect to claim 10, Takashi et al. a semiconductor device comprising (see figs. 1-6 and English abstract):

a) a semiconductor layer 3 that is provided over a layer (a p-n junction at the interface between 2 and 3) of electrically insulating material (since the p-n junction electrically insulates the bipolar transistors);

b) a plurality of first bipolar transistors 18,19 are provided in a first region over the semiconductor layer ;

c) a first isolation 4-1, 4-4 is provided over a main surface of the semiconductor layer to reach the layer of electrically insulating material;

d) a plurality of second bipolar transistors 20, 21 are provided in a second region over a portion of the semiconductor layer;

e) an second isolation 4-1, 4-4 is provided over a main surface of the semiconductor layer to reach the insulation layer;

wherein at least a portion of the plurality of first bipolar transistors is surrounded by the insulator layer and the first isolation the first region;

wherein at least a portion of the plurality of second bipolar transistors is surrounded by the insulator layer and the second isolation the second region;

wherein the surrounded first bipolar transistors operate substantially uniformly as constituent elements of a first unit transistor, and

wherein the surrounded second bipolar transistors operate substantially uniformly as constituent elements of a second unit transistor.

Takashi et al. fail to teach that the collectors, emitters, and bases of the first and second bipolar transistors are respectively connected in parallel with each other.

Kinoshita teaches collectors, emitters, and bases of a plurality of bipolar transistors are respectively connected in parallel with each other to achieve low-noise, high-power gain high frequency amplifier. See claim 1 and abstract.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Kinoshita into the device of Takashi et al. to attain the above benefit.

Further with respect to claim 10, Takashi et al. teach the electrically insulating layer is made of np junction layer but fail to teach the electrically insulating layer is made of material having lower thermal conductivity than the semiconductor layer or oxide.

Kitahara et al. teach using an oxide 13 to provide effective isolation for bipolar transistors.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Kitahara et al. into the device of Takashi et al. to attain the above benefit.

With respect to claims 11 and 12, Takashi et al. further fail to teach each of emitter of the plurality of first and second bipolar transistors is connected to a resistor made of polysilicon.

Moyer teaches connecting a polysilicon resistor to an emitter of a bipolar transistor to prevent thermal runaway. See col. 1, lines 35-40.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Moyer into the device of Takashi et al. to attain the above benefit.

With respect to claims 13, 14, and 15, Takashi et al. implicitly teach collector and base contact holes but fail to teach the range for the distance between contact holes for the base and collector of plurality of first and second bipolar transistors.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the distance between contact holes for the base and collector through routine experimentation and optimization to obtain optimal or desired device performance because in the absence of unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claims 16 and 17, Takashi et al. in combination with Kinoshita and Moyer fail to teach that the optimum current of the first bipolar transistor 1.5 times larger than the second bipolar transistor.

However, since Takashi et al. in combination with Kinoshita, Kitahara et al. , Moyer teach the claimed structure, the optimum current of the first bipolar transistor would be inherently be 1.5 times larger than the second bipolar transistor.

With respect to claim 18, Takashi et al. in combination with Kinoshita and Moyer fail to teach that the relative heat radiation and operation speed of the first bipolar transistor and the second bipolar transistor.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the relative heat radiation and operation speed of the first bipolar transistor and the second bipolar transistor through routine experimentation and optimization to obtain optimal or desired device performance because in the absence of unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Long Pham/

Primary Examiner, Art Unit 2814

/L. P./

Primary Examiner, Art Unit 2814